

# GX-AMC

Altera® Stratix® II GX AdvancedMC™



## Flexible, Fully-connected FPGA-based AdvancedMC

Based on Altera's Stratix II GX FPGA, BittWare's GX-AMC (GXAM) is a mid-size, single wide AdvancedMC that can be attached to AdvancedTCA (Advanced Telecom Compute Architecture) carriers or other cards equipped with AMC bays, and used in MicroTCA systems. The GXAM features a high-density Altera Stratix II GX FPGA, BittWare's ATLANTIS framework (implemented in the FPGA), a front panel I/O interface, a control plane interface via BittWare's FINE interface bridge, an IPMI system management interface, and a configurable 11x SerDes interface supporting a variety of protocols. It also provides 10/100 Ethernet, Gigabit Ethernet, two banks of DDR2 SDRAM, one bank of QDR2 SRAM, and Flash memory for booting the FPGA and FINE.

### Altera Stratix II GX FPGA

At the heart of the GXAM is a state-of-the-art Altera Stratix II GX FPGA which has been specifically designed for serial I/O-based applications providing up to 19 full-duplex high-performance, multi-gigabit transceivers supporting PCI Express, XAUI, Gigabit Ethernet, Serial RapidIO, and SerialLite II standards. It contains up to 132,540 equivalent LEs, over 6.7 Mbits of RAM, 252 embedded 18x18 multipliers, 63 DSP blocks, and 8 PLLs. BittWare's ATLANTIS framework, which enables seamless routing of the I/O, is implemented in the FPGA.

### Fat Pipes, Common Options, and I/O Interfaces

The Altera Stratix II GX FPGA facilitates all off-board I/O and provides communications routing and processing. Efficient routing is achieved using BittWare's ATLANTIS framework, which tightly integrates the I/O peripherals and the FPGA, and allows any combination of serial ports and off-board I/O interfaces to be routed together, providing nearly infinite options for configuring the I/O.

The Stratix II GX interfaces to three ports (1, 2, & 3) in the AMC common options region\*, and eight ports in the AMC fat pipes (4 - 11). These 11 ports provide a network data and control switch fabric interface on the AMC connector, configurable to support PCI Express, Serial RapidIO, GigE, or XAUI.

BittWare's FINE Bridge provides Gigabit Ethernet on port 0 of the common options region. It also provides 10/100 Ethernet and RS-232 on the AMC front panel.

The Stratix II GX provides four SerDes and 76 pairs of LVDS I/O to the BittWare front-panel I/O module, and 16 LVDS pairs (8 IN, 8 OUT) are provided for rear panel I/O via the AMC connector (ports 12 - 15, and 17 - 20). All AMC clocks are also connected to the Stratix II GX.

The GXAM implements the standard Module Management Control Interface (IPMI).

### Available Software

BittWare offers a complete suite of software development tools to make developing and debugging applications for the GXAM easy and efficient.

## Features

- Mid-size, single wide, fully-connected Advanced Mezzanine Card
  - ◆ Common Options region has four ports: port 0 provides Gigabit Ethernet, ports 1, 2, & 3 connect to BittWare's ATLANTIS framework\*
  - ◆ Fat Pipes region has eight ports: ports 4-11 configurable to support Serial RapidIO™, PCI Express™, GigE, and XAUI™ (10 GigE)
  - ◆ Rear panel I/O has eight ports (8 LVDS IN, 8 LVDS OUT)
  - ◆ System synchronization via AMC system clocks
  - ◆ Module Management Control (MMC) implementing IPMI
- High-density Altera® Stratix® II GX FPGA
  - ◆ BittWare's ATLANTIS framework for control of I/O, routing, and processing
  - ◆ 19 full-duplex SerDes transceivers
  - ◆ Up to 132,540 equivalent LEs
  - ◆ 252 embedded 18x18 multipliers and 63 DSP blocks
  - ◆ 6.7 Mbits of RAM
  - ◆ IP available for: Serial RapidIO™, PCI Express™, GigE, XAUI™ (10 GigE), CPRI, and OBSAI
- BittWare's FINE bridge provides control plane processing and interface via GigE, 10/100 Ethernet, and RS-232
- Over 1 GByte of memory
  - ◆ Two banks of DDR2 SDRAM (up to 512 MBytes each)
  - ◆ One bank of QDR2 SRAM (up to 9 MBytes)
- Front panel I/O
  - ◆ 10/100 Ethernet
  - ◆ RS-232
  - ◆ JTAG port for debug support
  - ◆ 4x SerDes (optional fiber adapter available)
- BittWare I/O Module: 76 LVDS pairs, 4 SerDes, Clocks, I2C, JTAG, DIO
- Booting of FINE and FPGA via Flash nonvolatile memory

\*Only available on the EP25SGX130



# GX-AMC Specifications

## BOARD ARCHITECTURE

### FPGA

- Altera Stratix II GX (EP2SG90/130)
- Up to 19 full-duplex, high-performance, multi-gigabit SerDes transceivers
- Up to 132,540 equivalent LEs
- Over 6.7 Mbits of RAM
- Up to 63 DSP blocks
- Up to 252 embedded multipliers
- 8 PLLs

### External Memory

- Two banks of up to 512 MBytes DDR2 SDRAM configured as x32
- One bank of up to 9 MBytes QDR2 SRAM configured as x36
- 64 MBytes of Flash memory for booting Stratix II GX and FINE

### Fat Pipes Interface

- Eight ports (4 - 11) @ up to 3.125 GHz configurable to support PCI Express, Serial RapidIO, GigE and XAU1

### Common Options Interface

- FINE™ bridge providing Gigabit Ethernet on port 0
- Ports 1, 2 & 3 via ATLANTIS framework, configurable to support PCI Express, Serial RapidIO, GigE, XAU1, and Serial ATA\*

### Other AMC Edge Connections

- All AMC clocks brought to ATLANTIS
- Module Management Control (MMC) Interface implementing IPMI for temperature monitoring and hot-swap support
- Eight ports providing 8 LVDS IN and 8 LVDS OUT

### AMC Front Panel I/O

- 10/100 Ethernet via FINE
- RS-232 port
- JTAG debug interface to the Stratix II GX
- Four SerDes @ up to 3.125 GHz (optional fiber adapter available)

### BittWare I/O Module

- Supports customizable front-panel I/O
- 76 LVDS pairs (38 In and 38 OUT)
- Clocks, I2C, JTAG, and DIO signals
- Four SerDes @ up to 3.125 GHz

### Power

- 25 W typical

### Size

- AMC mid-size, single width compatible with AMC specification R2.0

## SOFTWARE SUPPORT

### Host Interface

- BittWare's software development kit for Windows® and Linux contains C-callable libraries for board control and communications routines
- Porting kit available for other operating system platforms

### Development Tools

- Altera's Quartus® II software
- BittWare's FPGA Developers Kit with modules for ATLANTIS framework (I/O, routing, and processing), memory interfacing, and DMAs

## Ordering Information

GXAM-RW-AAB-CDE-FG

RW: Ruggedization

D: Memory Bank 2

0U = Commercial, 0°C to 50°C

0 = Not populated

AA: FPGA Size\*\*\*

7 = 256 MB DDR2 (default)

8 = 512 MB DDR2\*\*

90 = Stratix II GX 90

13 = Stratix II GX 130 (default)

E: Memory Bank 3

0 = Not populated

B: FPGA Speed Grade \*\*\*

7 = 256 MB DDR2 (default)

8 = 512 MB DDR2\*\*

4 = Speed grade 4 (default)

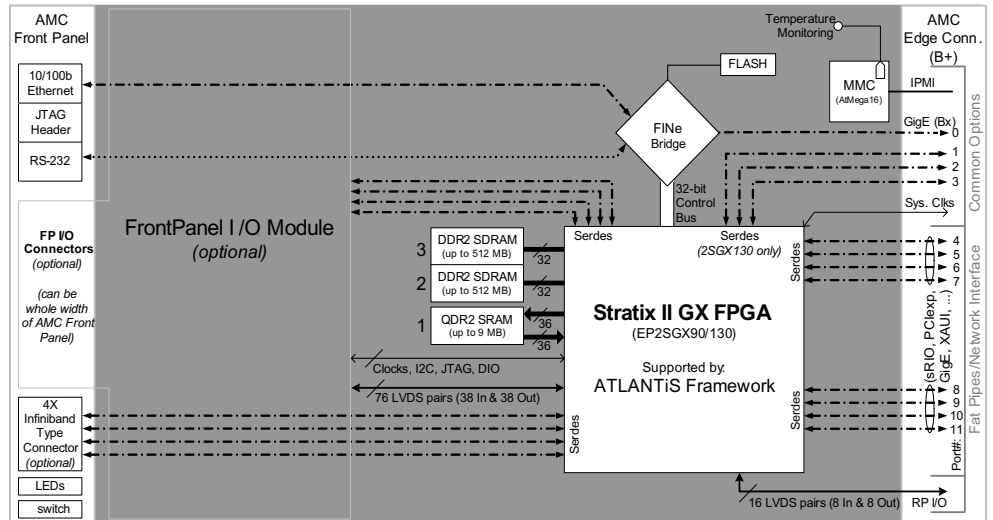
C: Memory Bank 1

FG: Front Panel Options

0 = Not populated (default)

F1 = Full size, standard cutouts

2 = 9 MB QDR2\*\*



\* Only available on the EP2SGX130

\*\* Contact BittWare for availability

\*\*\* Breakout board (GXBO) required for Altera FPGA JTAG debug