



iSPAN[™] 4576 Communications Interface

Technical Product Brief



Overview

The Interphase *iSPAN*[™] 4576 ATM over OC-3/STM-1 Communication Interface achieves high-performance through its on-board ATM protocol processing architecture that delivers an effective solution for both workstation and server applications. It also supports up to 64 K Virtual Connections (VCs) and provides full support for VBR, CBR, and UBR traffic in hardware.

The 32-bit, 33 MHz PCI interface provides the bandwidth necessary to continuously send and receive ATM SONET frames at 155 Mbps rate.

Main Features

The main characteristics of the Interphase *iSPAN* 4576 ATM over OC-3/STM-1 Communications Interface are as follows:

PCI

- 32-bit, 33 MHz PMC compliant adapter
- PCI Rev 2.1 with universal (3.3 V or 5 V signaling)
- PCI bus slave features:
 - 32-bit, address decoded with medium speed device
 - Memory and Configuration Read & Write cycles supported
 - Single access only, no bursting
- PCI bus master features:
 - 32-bit, zero wait transfers for up to 132 MBps burst DMA rate
 - 512x32-word Receive FIFO and 16x36-word Transmit FIFO buffering
 - Burst sizes up to thirteen 32-bit words for read, and fourteen 32-bit words for write

ATM

- Single OC-3/STM-1 capable SAR, single or dual PHY
- Physical interface for 155 Mbps optical transceiver with SC connector
- 256-byte receive FIFO, variable-length transmit FIFO, one to nine cells
- 4 MB (optional 8 MB) of on-board memory for storage of ATM connection parameters
- 32 K VCs (optional 64 K VCs) simultaneous full-duplex connections
- AAL0 and AAL5 adaptation layers:
 - AAL0: Single- or multi-cell frames
 - AAL5: Encapsulation provided in hardware
- OAM F4/F5 frame support
- Constant Bit Rate (CBR), Variable Bit Rate (VBR), and Unspecified Bit Rate (UBR) classes of service
- Automatic Protection Switching (APS) (device-level support for Class 1+1)

Platforms

- VxWorks[®] (5.4) API for PowerPC[™]
- Solaris[™] (2.7-2.9) API for SPARC[™] 32/64
- Linux[®] (2.4)
 - API for Intel[®] and PowerPC
 - ATM Miniport for Intel and PowerPC

Optional Features

- Single ATM connection, or redundant two connections
- On-board memory size (4 or 8 Mbytes)
- Optical transceivers with ST connectors
- Multimode/Single mode fiber

Configuration Options

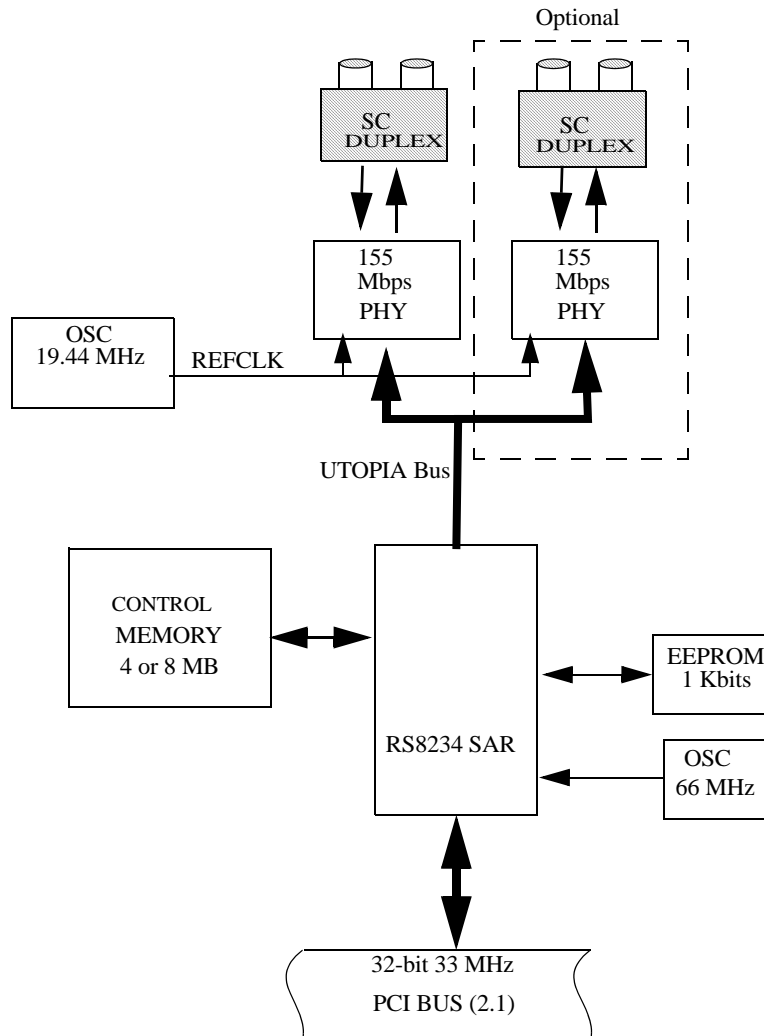
The following configurations are currently available:

- 4576-004:** SC duplex connector, Multimode fiber (62.5/125), up to 32 K VCs
- 4576-005:** SC duplex connector, Multimode fiber (62.5/125), up to 32 K VCs, Automatic Protection Switching (APS)
- 4576-006:** SC duplex connector, Single mode fiber (10/125) (intermediate reach), up to 32 K VCs
- 4576-007:** SC duplex connector, Single mode fiber (10/125) (intermediate reach), up to 32 K VCs, Automatic Protection Switching (APS)

Contact your Interphase representative for custom configurations.

Hardware Description

Block Diagram



Mindspeed RS8234 ATM SAR

- Conforms to the ATM Forum recommendations
- 32-bit 33 MHz PCI 2.1 compliant with universal signaling
- UTOPIA 1 interface, with two PHY chip selects
- 32-bit local bus interface
- Up to 64 K of total Virtual Channels
- Hardware support for CBR, VBR, and UBR services

INTERPHASE PROPRIETARY

- OAM F4/F5 frame support

Mindspeed CX28250 PHY

- Meets ATM Forum standards
- 155 Mbps full duplex operation
- OC-3/STM-1
- UTOPIA 1 bus interface

Optical Transceiver

- 1X9 form factor
- SC connector (Contact Interphase for other connectors.)
- Multimode 1300 nm LED for short range (< 2 km)
- Single mode 1300 nm LASER for intermediate range (<15 km) or long range (40 km)

Controller Functions

PCI Bus

- Complies to PCI Revision 2.1 specification for 32-bit, 33 MHz environment.
- Universal signaling
- 3.3 V and 5 V

UTOPIA Interface

- UTOPIA 1 bus
- UTOPIA signals are shared between two PHY devices

Control Memory

The *iSPAN* 4576 uses the control memory to store parameters for segmentation and reassembly. The maximum size of the control memory is 8 MBytes for up to 64 K VCs.

Environmental and Mechanical

Powered by +3.3 V and +5 V available from the PMC connectors.

	3.3 V	5.0 V	Total
Single PHY	0.30 A	0.61 A	4.5 W
Dual PHY	0.35 A	1.07 A	7.0 W

The *i*SPAN 4576 conforms to PMC IEEE1386.1 Draft 2.4:

- Length: 5.87 inches/149 mm
- Width: 2.91 inches/74 mm

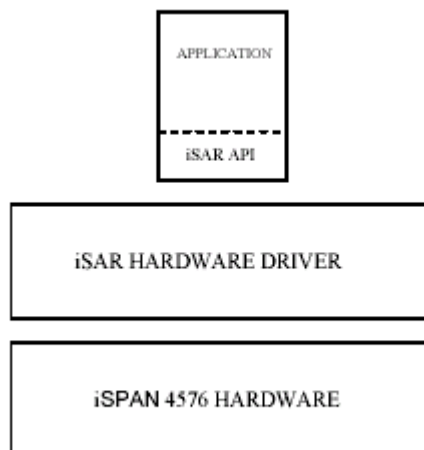
***i*SAR Application Programming Interface (API)**

The *i*SAR API provides a seamless, robust interface between an application and the underlying hardware, isolating the application from dealing directly with the complexity of the hardware, simplifying the application development process.

The API is implemented as a series of synchronous messages exchanged between the application and API. These messages are divided into four main groups:

- Query
 - Current state, configuration, and statistical information
- Control
 - Configuration, management, and flow control
- Connections
 - Set-up/tear-down
 - Transmit/receive
- Alarms
 - PCI
 - SAR
 - Data
 - Line

The *i*SAR API data path is through the API, not the native host interface (i.e., streams or sockets). Asynchronous events such as receive data and alarm indications are executed via user-specified callback functions.



Automatic Protection Switching

The RS8234 SAR has a UTOPIA 1 bus, with two PHY chip selects. In conjunction with the CX28250 PHYs, the second PHY chip select allows the second PHY to share the same UTOPIA bus for APS capability. Both PHYs transmit and receive all data. Both PHYs receive data from the redundant network, but only the primary PHY transfers data back to the ATM SAR. APS operating parameters and event notification are available through the API, including the selection of active and/or protective PHY.

The receive outputs of the protective PHY are in high impedance state.

Interphase provides the *iSPAN 4576* in two basic configurations to support APS operation:

- Single PHY for 1:n implementation
- Dual PHY for 1+1 implementation

Software Package

Each of the supported platform software packages includes the following components:

- Low level driver (binary)
- Associated API library (binary)
- Configuration, diagnostic, and troubleshooting tools (binary)
- API header files: Required for application development
- Sample configuration file
- Functional sample source of diagnostic utilities
- Users documentation: Documentation includes details on installing the 4576 hardware module, an overview of the API, and detailed information regarding each API function call

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