The Embedded I/O Company

TEWS TECHNOLOGIES

TIP811

INTERBUS Master G3 Interface

Version 1.0

User Manual

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TIP811-10

INTERBUS Master G3 Interface

TIP811-TM-10

Transition Module for TIP811-10

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue with Firmware V1.0	September 1995
1.1	New Firmware V1.1 from Phoenix	March 1997
1.2	Add Mode Description	November 1998
1.3	General Revision	January 2004

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1 Product Description

The TIP811 is an IndustryPack® compatible module providing a complete INTERBUS master interface using a local MC68332 controller and the IPMS3 interface chip of PHOENIX CONTACT.

The original PHOENIX INTERBUS master firmware is running on the TIP811 local MC68332 controller, handling the complete INTERBUS communication protocol.

The PHOENIX CONTACT firmware revision used on the TIP811-10 V1.0 Rev. B supports two operating modes, Native Mode and Enhanced Mode. For both modes interrupt support can be activated.

After power-on or reset the Native Mode is active. This mode is fully function compatible with firmware revision 1.0 used on the TIP811-10 V1.0 Rev. A.

The IBS SYS SWT INTERBUS configuration software (PHOENIX CONTACT) can be used in Native Mode.

The TIP811 can be switched to the Enhanced Mode. In Enhanced Mode the following new features are supported:

- handshake controlled communication by mailboxes
- up to 32 INTERBUS PCP modules with PCP1.5 (1 word PCP)
- support for the IBS CMD INTERBUS configuration software (PHOENIX CONTACT)

The communication between the host CPU, the TIP811 and the INTERBUS is handled via Dual Port RAM memory areas.

Software Driver support (TIP811-SW-xx) is available for various operating systems.

The TIP811-TM-10 transition module is required for the TIP811. It provides the optically isolated INTERBUS I/O interface, a RS232 diagnostic port and status LEDs.

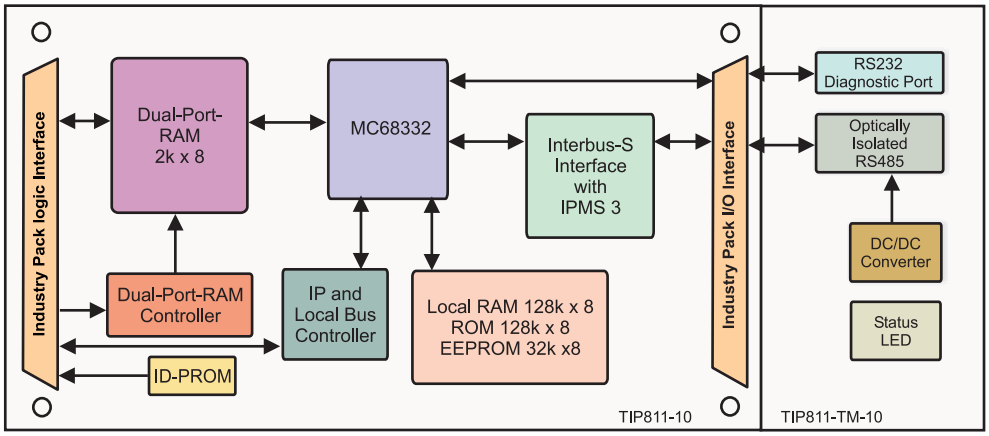


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
Identification PROM	Supports auto configuration	
ID ROM Data	Format I / no wait states	
I/O Space	Used / no wait states	
Memory Space	Used / 1 wait state	
Interrupts	Intreq0# used (DPM) / Intreq1# used (Service)	
DMA	Not supported	
Clock Rate	8MHz	
Module Type	Type I	
Local Bus Controller	MC68332	
INTERBUS Controller	IPMS-3 Physical and logical addressing 64 remote bus segments maximum 128 number of modules maximum 2048 I/O maximum EEPROM supported 32 PCP modules maximum (PCP V1.5, 1 word PCP) Mailboxes supported in Enhanced Mode	
Operating Modes	Native Mode (Identical with firmware 1.0 used on the TIP811-10 V1.0 Rev. A) Enhanced Mode	
System Control	Bit controlled by 8 factory installed sequences Handshake controlled communication by mailboxes in Enhanced Mode	
I/O Interface		
Interface Connector	50-conductor flat cable	
Diagnostic	LED, Dual Port Memory (DPM) and V.24	
Transition Module	TIP811-TM-10 required, provides isolation for remote INTERBUS, signal conditioning for V.24 and diagnostic LEDs	
Physical Data		
Power Requirements	250mA typical @ +5V DC for TIP811-10 with Transition Module TIP811-TM-10	
Temperature Range	Operating Storage	0 °C to +70 °C -45°C to +125°C
MTBF	333897h	
Humidity	5 – 95 % non-condensing	

Figure 2-1 : Technical Specification

3 ID Prom Contents

Offset	Function	Value
0x01	ASCII ‘I’	0x49
0x03	ASCII ‘P’	0x50
0x05	ASCII ‘A’	0x41
0x07	ASCII ‘C’	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x16
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low - Byte	0x00
0x13	Driver-ID High - Byte	0x00
0x15	Number of bytes used	0x0D
0x17	CRC	0xA8
0x19	Version -10	0x0A

Figure 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP811 is accessible in the IP I/O space.

Offset	Symbol	Description	Size (Bit)	Access
0x01	CNTSR	Control and Status Register	8	R/W
0x03	ENAINT	Interrupt Enable Register	8	R/W
0x05	INTVEC	Interrupt Vector Register	8	R/W

Figure 4-1 : Register Set

4.2 Control and Status Register (CNTSR)

The bits are automatically cleared with the IP_Reset# signal.

Bit	Symbol	Description	Access	Reset Value
7		Always read as '0'.		
6	SVC IRQ	Status Service Interrupt Request The service interrupt is generated upon detection of a hardware error (no oscillation, watchdog, etc.) Read : 0 : No interrupt request pending 1 : Interrupt request pending Write : Writing a '1-0' sequence clears the service interrupt request	R/W	0
5	DPM IRQ	Status DPM Interrupt Request The DPM interrupt is generated if the local MC68332 controller writes to DPM location 0x7FE. Read : 0 : No interrupt request pending 1 : Interrupt request pending Write : No effect The DPM interrupt request is acknowledged by the host with a read access to DPM location 0x7FE.	R/W	0
4:2		Always read as '0'.		
1	RESET	MC68332 (local controller) Reset Read : 0 : Reset is not active 1 : Reset is active Write: 0 : Release MC68332 from reset state 1 : Force MC68332 into reset state	R/W	0
0	CAO INS	Clear_All_Outputs Instruction for MC68332 (local controller) Read : 0 : Clear_All_Outputs instruction not active 1 : Clear_All_Outputs instruction active Write : 0 : Releases the Clear_All_Outputs state. The local MC68332 controller updates its local buffer with the next INTERBUS cycle. The INTERBUS outputs are updated with these values. 1 : Forces the local MC68332 controller to clear the OUT_DATA area of the DPM, to copy the OUT_DATA area to the local buffer, and to start an INTERBUS cycle to transfer the cleared OUT_DATA area from the local buffer to the INTERBUS outputs. As long as this bit is '1', all outputs on the INTERBUS remain cleared. New data can be written by the host to the OUT_DATA area of the DPM, but the local MC68332 controller does not copy the DPM OUT_DATA area to the local buffer. The local MC68332 controller uses the cleared local buffer area for the INTERBUS outputs.	R/W	0

Figure 4-2 : Control and Status Register (CNTSR)

After power-on or reset, the local MC68332 controller clears the Indication Register TIP811 in the DPM before starting the Power On Self Test (POST).

This write access to the Indication Register TIP811 initiates a DPM interrupt request to the host system!

The host should clear this interrupt request by reading DPM location 0x7FE before starting any other activities.

4.3 Interrupt Enable Register (ENAINT)

The bits are automatically cleared with IP_RESET# signal.

Bit	Symbol	Description	Access	Reset Value
7		Don't care for writes. Always read as '0'.		
6	SVC INTEN	This bit controls the interrupt enable for the service request interrupt. 0 : Service interrupt disabled 1 : Service interrupt enabled	R/W	0
5	DPM INTEN	This bit controls the interrupt enable for the DPM interrupt. 0 : DPM interrupt disabled 1 : DPM interrupt enabled	R/W	0
4:0		Don't care for writes. Always read as '0'.		

Figure 4-3 : Interrupt Enable Register (ENAINT)

4.4 Interrupt Vector Register (INTVEC)

Bit	Symbol	Description	Access	Reset Value
7:0	INT_VEC	Interrupt Vector loaded by software. Write data for bit 0 is ignored. For interrupt vector read, bit 0 indicates the interrupt request line. Bit 0 read as '0' : Interrupt on Intreq0# (DPM interrupt) Bit 0 read as '1' : Interrupt on Intreq1# (Service interrupt) E.g. If the register is loaded with 0x60, DPM interrupt will create an interrupt vector 0x60 and Service Request will create an interrupt vector 0x61.	R/W	0x00

Figure 4-4 : Interrupt Vector Register (INTVEC)

The DPM interrupt is mapped to the INTREQ0# interrupt request line and the Service Request interrupt is mapped to the INTREQ1# interrupt request line of the IP bus.

5 Memory Space Addressing

The TIP811 is accessed in the IP memory space via a Dual Port Memory (DPM) of 2 x 8Kbyte. Address range : IP_memory_base_address + (0x000 to 0x7FF).

The new PHOENIX CONTACT firmware revision 1.1 used on the TIP811-10 V1.0 Rev. B supports two operating modes, Native Mode and Enhanced Mode. The address map of the TIP811 DPM space depends on the selected operating mode.

After power-on or reset the Native Mode is active. This mode is fully function compatible with firmware revision 1.0 used on the TIP811-10 V1.0 Rev. A.

The TIP811 can be switched to the Enhanced Mode. In Enhanced Mode the following new features are supported:

- handshake controlled communication by mailboxes
- up to 32 INTERBUS PCP modules with PCP1.5 (1 word PCP)
- support for the IBS CMD PHOENIX CONTACT INTERBUS configuration software

5.1 Native Mode Address Map

In Native Mode the Dual Port Memory is divided into 4 areas:

INTERBUS Out_Data	(0x000 to 0x0FF)
INTERBUS In_Data	(0x100 to 0x1FF)
INTERBUS Message Area	(0x200 to 0x3DF)
Register Area	(0x3E0 to 0x7FF)

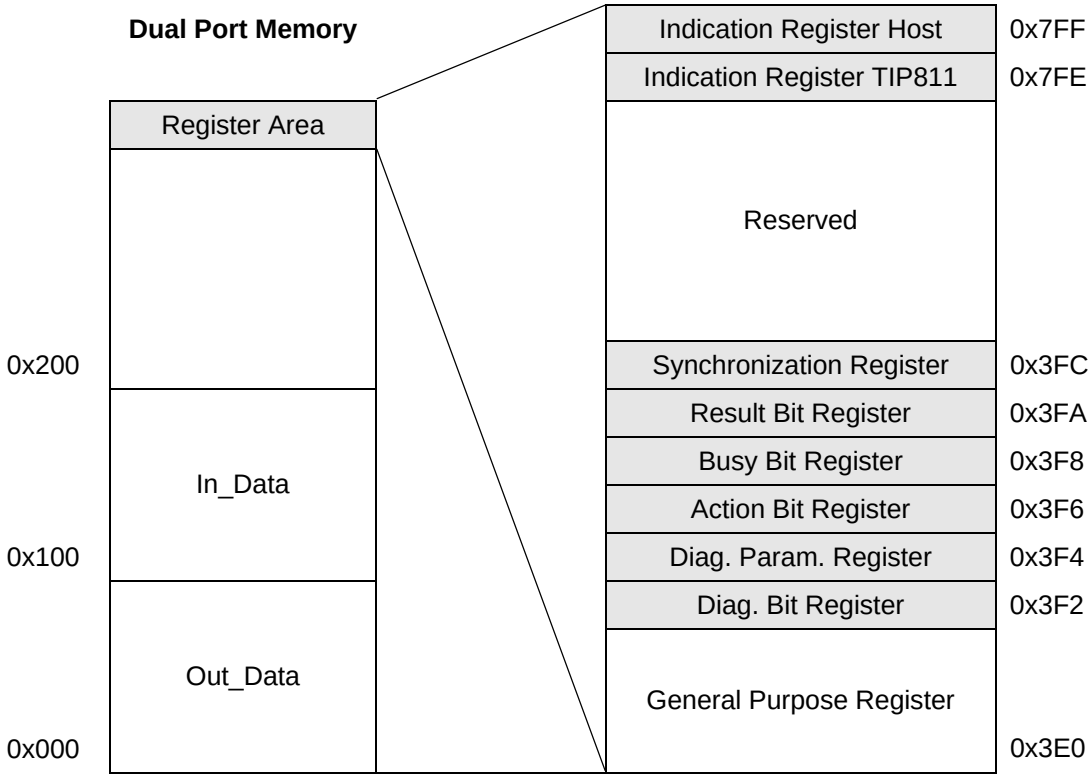


Figure 5-1 : Dual Port Memory Address Map in Native Mode

5.2 Enhanced Mode Address Map

In Enhanced Mode the Dual Port Memory is divided into 5 areas:

INTERBUS Out_Data	(0x000 to 0x0FF)
INTERBUS In_Data	(0x100 to 0x1FF)
Mailbox Host -> TIP811	(0x200 to 0x47F)
Mailbox TIP811 -> Host	(0x480 to 0x6FF)
Register Area	(0x700 to 0x7FF)

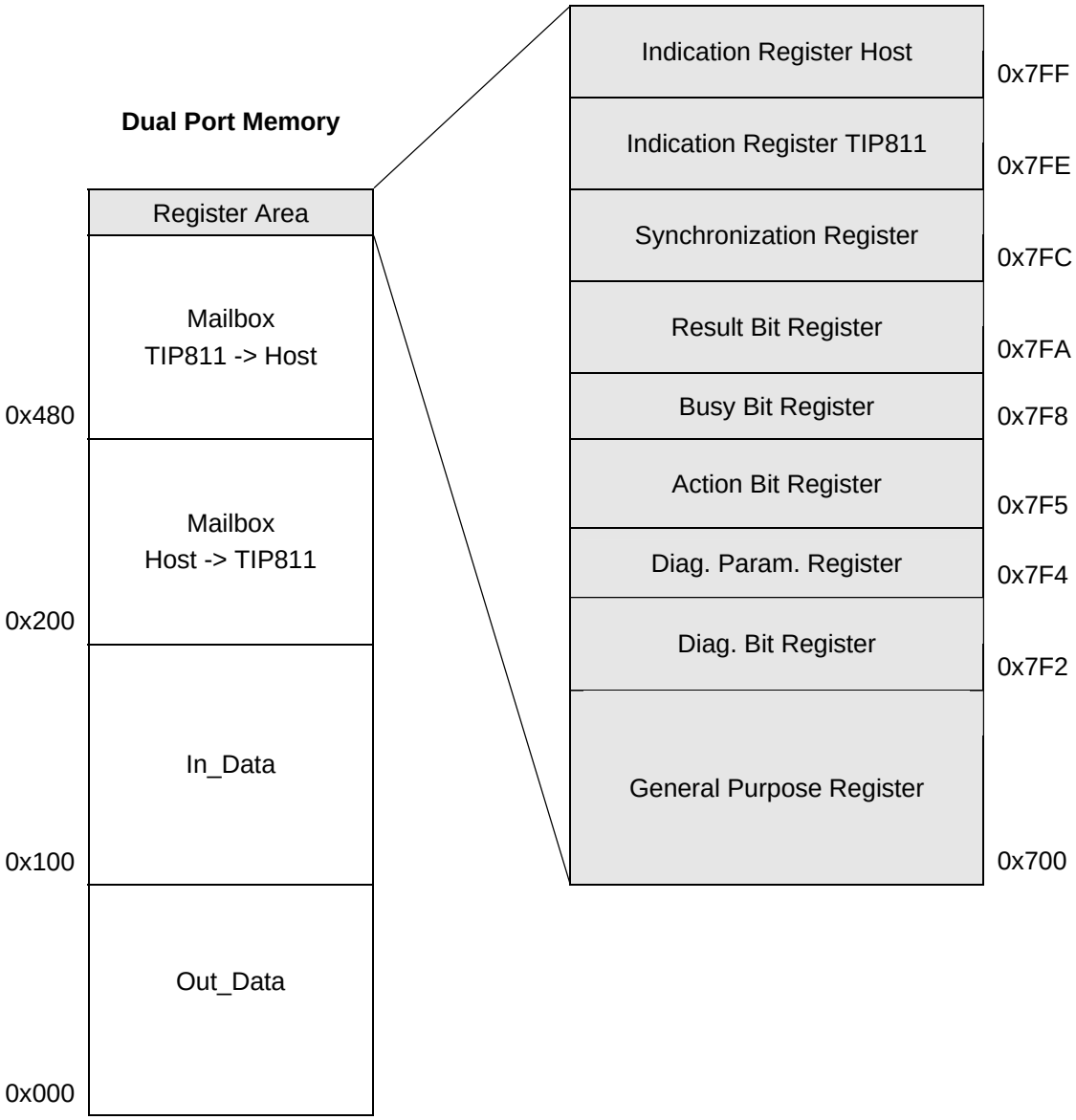


Figure 5-2 : Dual Port Memory Address Map in Enhanced Mode

5.3 Register Area

5.3.1 General Purpose Registers

The General Purpose Registers can be used by the host. For both operating modes, the General Purpose Register areas are not tested or initialized by the local MC68332 controller.

5.3.2 Diagnostic Bit Register

The Diagnostic Bit Register contains information about the current state of the INTERBUS and the TIP811. Only the TIP811 updates this register.

Bit	Symbol	Description	Access	Reset Value
15		Reserved	R	
14	QUALITY	1 = more than 20 of 1 million INTERBUS cycles corrupted	R	
13:8		Reserved	R	
7	READY	1 = TIP811 Ready	R	
6	FAIL	1 = Host Error	R	
5	RUN	1 = INTERBUS Cycles Running	R	
4	BSA	1 = Bus Segment Switched Off	R	
3	CTR	1 = TIP811 Controller Error	R	
2	RB	1 = Remote Bus Error	R	
1	LB	1 = Local Bus Error	R	
0	MOD	1 = Module Error	R	

Figure 5-3 : Diagnostic Bit Register

5.3.3 Diagnostic Parameter Register

The Diagnostic Parameter Register contains the number of modules connected to the INTERBUS (bits 15:8) and an error code for the last error (bits 7:0). This register is updated by the TIP811 only.

Bit	Symbol	Description	Access	Reset Value
15:8		Module Count	R	
7:0		Error Code	R	

Figure 5-4 : Diagnostic Parameter Register

5.3.4 Action, Busy and Result Bit Register

The Action Bit Register, Busy Bit Register and Result Bit Register are used to control the INTERBUS by the mechanism of bit controlled command execution. Bit controlled command execution is available in both operating modes, Native Mode and Enhanced Mode.

Each bit of the Action Bit Register can be assigned an INTERBUS command sequence (one or several INTERBUS commands).

See chapter “Command Sequences” for a list of the eight predefined INTERBUS command sequences.

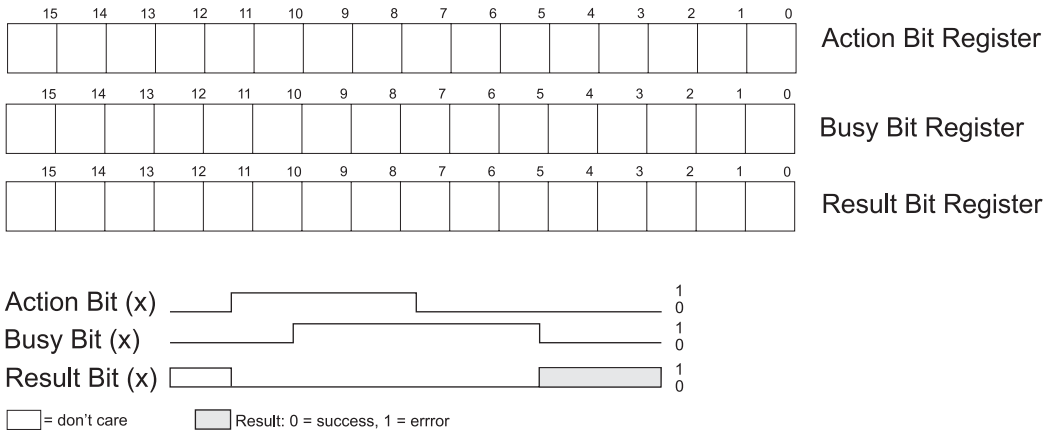


Figure 5-5 : Bit Controlled Command Execution

Setting a bit in the Action Bit Register by the host initiates the execution of the command sequence assigned to this bit.

The local MC68332 controller sets the according bit in the Busy Bit Register when it starts with the execution of the requested command sequence and clears the according bit in the Result Bit Register. Busy Bit and Result Bit Register are updated by the TIP811 only.

The host clears the action bit when it detects that the busy is set. Now the host waits for the busy bit to clear and then checks the result bit.

A new action is allowed to be started after completion of the sequence described above.

5.3.5 Synchronization Register

The Synchronization Register is used to exchange I/O data between the host and the TIP811. By the use of the Synchronization Register it is possible to exchange more than 8 bit of I/O data consistently.

The host first writes all data to the Out_Data area of the Dual Port memory (DPM) and then writes the value 0xAA55 to the Synchronization Register. Now the local MC68332 controller copies all data from the Out_Data area to an internal buffer from which the data is transferred to the INTERBUS with an INTERBUS cycle. When the INTERBUS cycle is completed, the local controller copies all actual INTERBUS In_Data from a local buffer to the In_Data area of the DPM and then sets the Synchronization Register to 0x55AA.

If polling mode is active, don't write to the Indication Register Host.

5.3.6 Indication Register TIP811

The Indication Register TIP811 is a special register in the DPM (address 0x7FE). Each time the local MC68332 controller writes to this register, an interrupt to the host is initiated (if bit 5 of the Interrupt Enable Register is set). The interrupt request is cleared by a host read access to this register.

For both operating modes, Native Mode and Enhanced Mode, interrupt support can be enabled. Enabling interrupt support must follow directly after selecting the operating mode. If interrupts are enabled, the TIP811, upon changes in the Synchronization Register, the Busy Bit Register and the Diagnostic Bit Register) sets the according bits (0, 2, 3) in the Indication Register TIP811.

A bit in the Indication Register TIP811 is only set by the local MC68332 controller if the Indication Register TIP811 is '0'. To avoid an indication overrun it is necessary for the host to clear the Indication Register TIP811 by a read access within a predefined timeout of 200ms. Otherwise a controller error (code 0x0C) will be generated by the local MC68332 controller and bit 3 of the Indication Register TIP811 is forced to '1'.

If interrupt support is disabled all bits except bit 7 have no function.

The TIP811 writes to the Indication Register TIP811 in interrupt mode only.

Bit	Symbol	Description	Access	Reset Value
7		Handshake Bit TIP811 ('1' = new message in mailbox TIP811 -> Host)		
6:4		Reserved		
3		Diagnostic Bit Register Modified		
2		Busy Bit Register Modified		
1		Reserved		
0		Synchronization Register Modified		

Figure 5-6 : Indication Register TIP811

5.3.7 Indication Register Host

The Indication Register Host is a special register in the DPM (address 0x7FF). Each time the host writes to this register, an interrupt to the local MC68332 controller is initiated. The local MC68332 acknowledges the indication by a read access to the Indication Register Host. This read access clears the Indication Register Host. The host must set a bit in the Indication Register Host only if this register is '0'. If interrupt support is disabled all bits except bit 7 have no function.

If polling mode is active don't write to the Indication Register Host.

Bit	Symbol	Description	Access	Reset Value
7		Handshake Bit Host ('1' = new message in mailbox Host -> TIP811)		
6:3		Reserved		
2		Action Bit Register Modified		
1		Reserved		
0		Synchronization Register Modified		

Figure 5-7 : Indication Register Host

5.4 Message Area

In Native Mode the DPM area (0x200) functions as the INTERBUS Message Area. After execution of an INTERBUS command the local MC68332 controller puts the message code that belongs to the INTERBUS command into the INTERBUS Message Area starting at address 0x200.

If an INTERBUS command sequence, which can consist of several INTERBUS commands is executed by the local controller, the Message Area holds the message code of the last executed INTERBUS command of the INTERBUS command sequence.

For a detailed summary of all message codes and formats please refer to the PHOENIX CONTACT IBS MA/B-T firmware manual.

5.5 Mailbox Area

In Enhanced Mode the DPM area (0x200 to 0x47F) functions as the INTERBUS Mailbox Host -> TIP811. The DPM area (0x480 to 0x6FF) functions as the INTERBUS Mailbox TIP811 -> Host.

5.6 In_Data

The INTERBUS In_Data area (0x100 to 0x1FF) reflects the actual state of all INTERBUS inputs. It is updated by the local MC68332 controller after each INTERBUS data cycle.

5.7 Out_Data

During each INTERBUS data cycle the local MC68332 controller updates the INTERBUS outputs with the data of the DPM INTERBUS Out_Data area (0x000 to 0x0FF). The DPM Out_Data area is updated by the host.

6 Command Sequences

The TIP811 contains an EEPROM which can take up to 16 INTERBUS command sequences.

Each INTERBUS command sequence consists of one or several INTERBUS commands.

Eight predefined INTERBUS command sequences are factory installed and executable.

Bit	INTERBUS Command Sequence	INTERBUS Commands
0	Start INTERBUS	Clear Display (0x004E) Configure Bus (0x0023) Start Bus Cycle (0x0001)
1	Read and check INTERBUS system	Clear Display (0x004E) Configure Bus (0x0023)
2	Clear Diagnostic Register and Error LEDs	Clear Display (0x004E)
3	Update module error (Diagnostic Register and LEDs)	Send All Module Error (0x005C)
4	Quit all module errors	Quit Module Error All (0x0065)
5	Stop INTERBUS and clear all outputs	Alarm Stop (0x004A)
6	INTERBUS System Stop and new Start Up	Warm Start (0x004C)
7	Read actual INTERBUS configuration	Send Physical Conf. (0x005E)

Figure 6-1 : Predefined INTERBUS Command Sequences

6.1 Programming Command Sequences

6.1.1 Native Mode

In Native Mode the IBS SYS SWT INTERBUS configuration software (PHOENIX CONTACT), running on a standard PC, can be used to program INTERBUS command sequences via the V.24 port of the TIP811-TM-10 Transition Module.

6.1.2 Enhanced Mode

The Enhanced Mode provides two ways to program INTERBUS command sequences:

- by command execution via the mailboxes
- by the IBS CMD INTERBUS configuration software (PHOENIX CONTACT).

7 Operating Modes

The PHOENIX CONTACT firmware revision 1.1 used on the TIP811-10 V1.0 Rev. B supports two operating modes, Native Mode and Enhanced Mode.

After reset or power-on the Native Mode is active. The mode is fully function compatible with firmware revision 1.0 used on the TIP811-10 V1.0 Rev. A.

The TIP811 can be switched to the Enhanced Mode. In this mode the following new features are supported:

- handshake controlled communication by mailboxes
- up to 32 INTERBUS PCP modules with PCP5.1 (1 word PCP)
- support for the IBS CMD INTERBUS configuration software (PHOENIX CONTACT).

Both operating modes, Native and Enhanced Mode support interrupts. Interrupt support must be selected directly after selecting the operating mode.

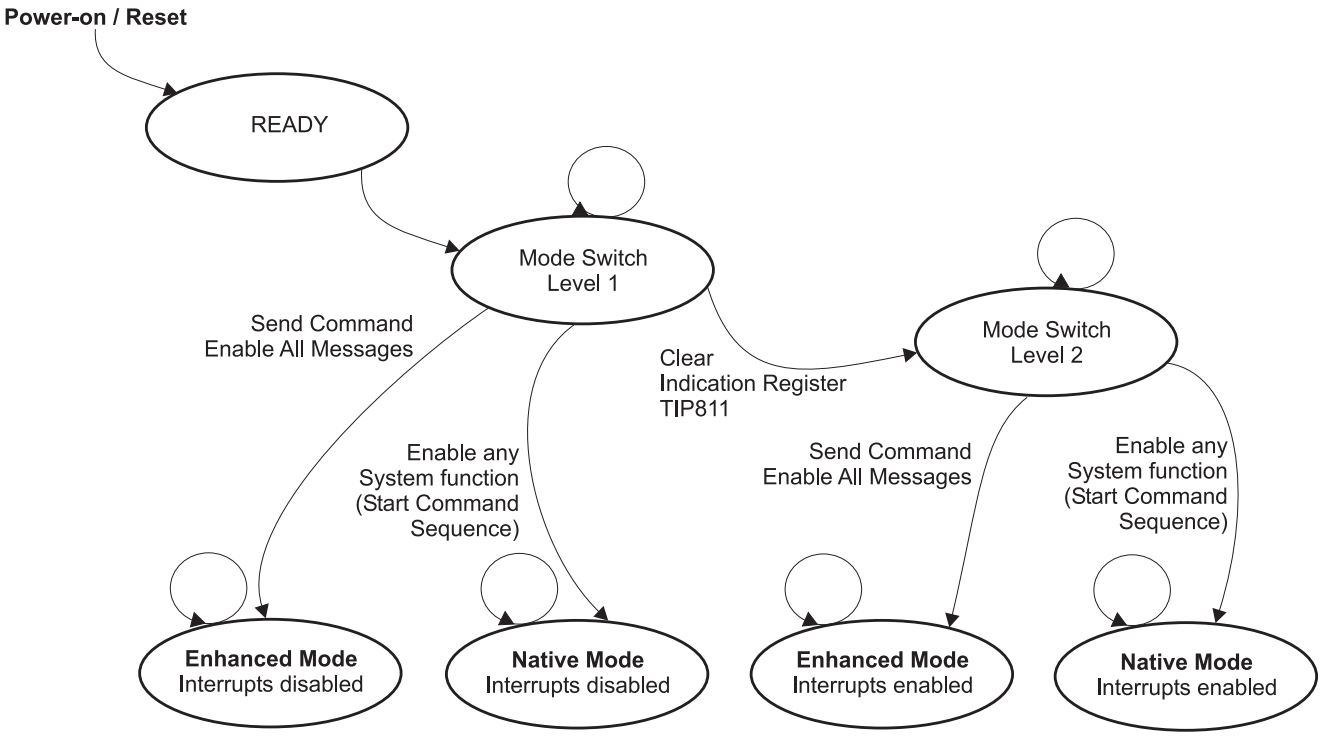


Figure 7-1 : Selection of Operating Mode

After reset or power-on the MC68332 controller clears the Indication Register TIP811 before starting the Power On Self Test (POST). This write access to the Indication Register TIP811 initiates a DPM Interrupt Request to the host system! The host should clear this interrupt request by reading DPM location 0x7FE before starting any other activities.

7.1 Synchronization after Power-On

To synchronize an application program running on the host system with the firmware running on the TIP811, the local MC68332 controller indicates 'READY' to the host after the Power On Self Test (POST) has finished, by setting the Ready bit in the Diagnostic Bit Register at address 0x3F2 and setting bit 3 of the Indication Register at address 0x7FE.

7.2 Select Enhanced Mode

In Native Mode it is always possible to switch to Enhanced Mode, but it is not possible to switch back to Native Mode. To switch to the Enhanced Mode the Indication Register TIP811 must be cleared by a read access from the host. Then the host writes the command Enable_All_Messages to 0x200 and sets bit 7 of the Indication Register Host. This command leads to the following action on the TIP811:

- set operating mode flag to Enhanced Mode
- run warm start
- check operating mode flag
- if first warm start after selecting Enhanced Mode then
    - o set READY bit in Diagnostic Bit Register (now at address 0x7F2)
    - o suppress message to host for command Enable_All_Messages.

7.3 Mailbox Protocol

Sending commands to the TIP811 and receiving messages from the TIP811 is shown in the following diagrams (viewed from the host). The mailbox protocol is only available in Enhanced Mode.

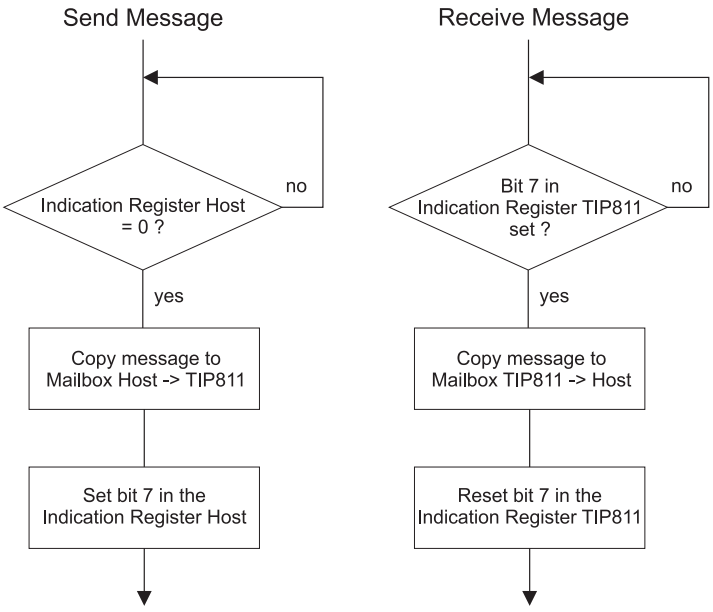


Figure 7-2 : Mailbox Protocol

7.4 Rules for I/O Data Exchange

After the operating mode has been determined, the host can start INTERBUS command sequences.

The Synchronization Register is used to exchange I/O data between the host and the TIP811. By the use of the Synchronization Register it is possible to exchange more than 8 bit of I/O data consistent.

The host first writes all data to the Out Data area of the Dual Port Memory (DPM) and then writes the value 0xAA55 to the Synchronization Register. Now the local MC68332 controller copies all data from the Out Data area to an internal buffer from which they are transferred to the INTERBUS by an INTERBUS cycle. When the INTERBUS cycle is completed the local controller copies all actual INTERBUS In Data from a local buffer to the In Data area of the DPM and then sets the Synchronization Register to 0x55AA.

The following rules apply for the addressing of I/O data in the In Data and Out Data area of the DPM:

- No difference between analog and digital data
- In Data is placed in the In Data area in ascending addresses without a gap.
- Out Data is placed in the Out Data area in ascending addresses without a gap.
- The starting address of both, In Data and Out Data starts with an address offset of ‘0’. Dummy bytes are not copied and no space is reserved for dummy bytes.
- Addresses of INTERBUS word modules can start at odd addresses.

7.5 Polling Mode

In polling mode the Indication Registers have no functions. The application program polls the Diagnostic Register, the Busy Bit Register, and the Sync. Register. Actions are started immediately after recognition of the registers mentioned.

7.6 Interrupt Mode

Changes in the Sync. Register, the Busy Bit Register, and the Diagnostic Registers are indicated to the application program by setting the bits 0, 2 and 3 in the Indication Register TIP811 (and thus by interrupt). The Indication Register TIP811 has to be cleared by the host within the given timeout (default 200ms). Manipulations of the Sync. Register and the Action Register by the host have to be indicated to the TIP811 by setting the bit 0 or bit 2 in the Indication Register Host.

8 Application Interface

The Application Interface (AI) is the interface between the host and TIP811. The AI is based on the Dual Port Memory. Two different AI's exist depending on the selected operating mode, Native Mode or Enhanced Mode.

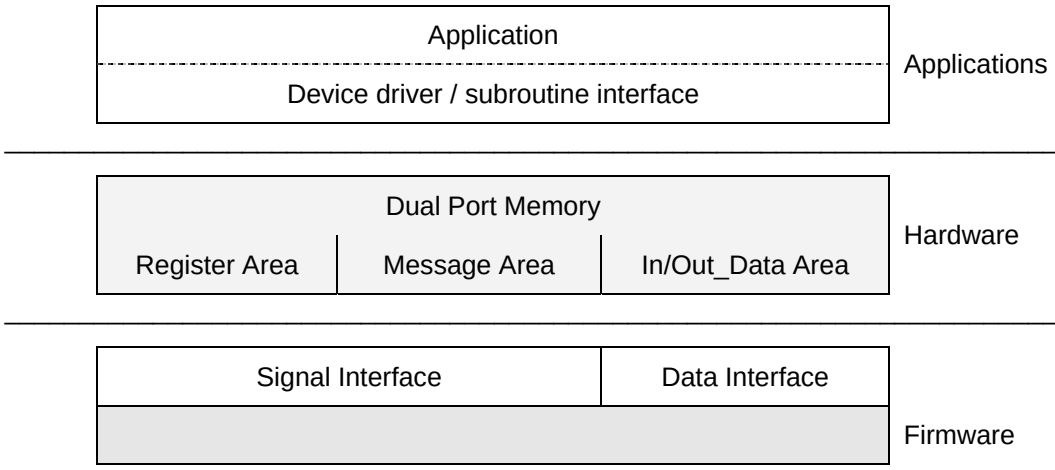


Figure 8-1 : Application Interface Native Mode

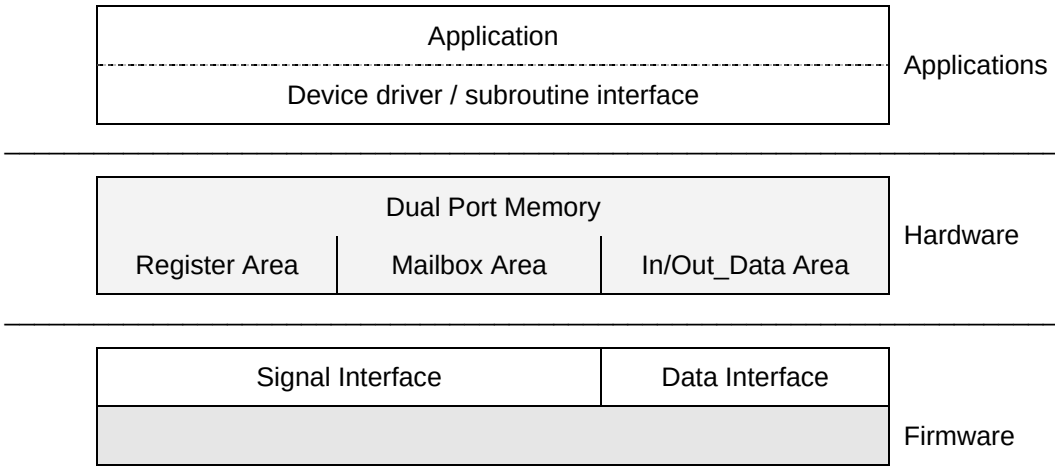


Figure 8-2 : Application Interface Enhanced Mode

9 Firmware

The original PHOENIX CONTACT IBS MA/B-T firmware runs on the TIP811.

The following diagram shows the different firmware states. For a detailed firmware description please contact PHOENIX CONTACT.

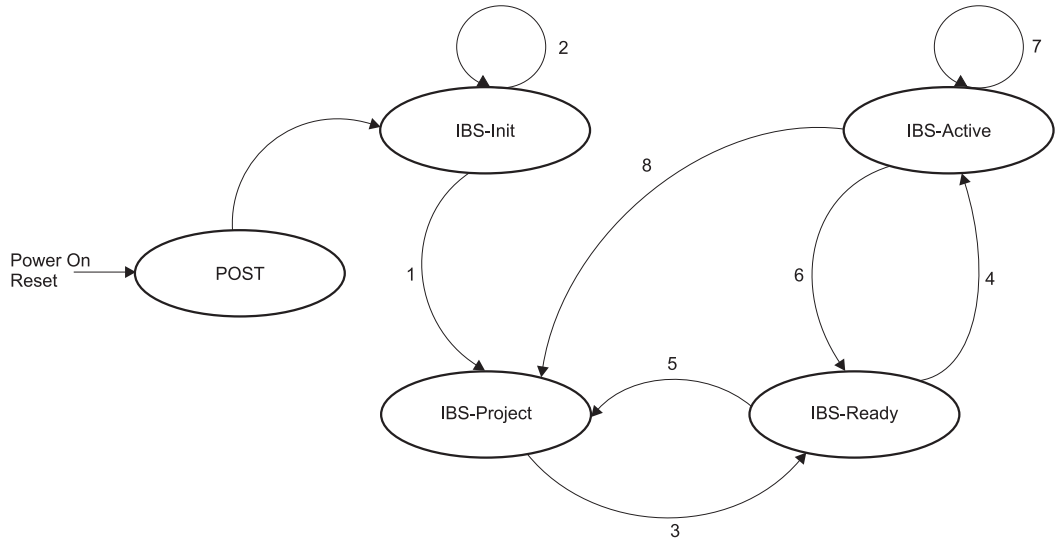


Figure 9-1 : Firmware States

States

POST	After power-on or reset the firmware enters a Power On Self Test (POST).
IBS-Init	Initialization of all hardware and firmware. This state is left only after successful initialization.
IBS-Projekt	The INTERBUS is not ready. No data cycles are running.
IBS-Ready	The INTERBUS is ready and can be started. No data cycles and no ID cycles are running.
IBS-Active	Data cycles are running as long as none of the following conditions occur: - Command Stop Bus Cycle - Command Alarm Stop - Command Warm Start - Multiple Transfer Error

State Transitions

POST -> **IBS- Init**	Self Test is completed successful.
IBS-Init -> **IBS-Init**	Error is occurred during initialization.
IBS-Project -> **IBS-Ready**	The INTERBUS is ready. A valid bus configuration exists.
IBS-Ready -> **IBS-Active**	Received Start Bus Cycle command
IBS-Ready -> **IBS-Project**	Received command to configure the INTERBUS (i.e. check physical configuration)
IBS-Active -> **IBS-Ready**	Received command to stop the INTERBUS
IBS-Active -> **IBS-Active**	The firmware stays in this state until a multiple bus error has happened or the bus has stopped.
IBS-Active -> **IBS-Project**	During a data cycle a local or remote bus error has happened.
Every state -> **IBS-Init**	Received Warm Start command

9.1 Power On Self Test (POST)

After power-on or reset a Power On Self Test (POST) is executed. The POST checks the hardware and executes the following steps:

- Start

  Initialization of system integration module of MC68332 controller

- m68000_self_test

  MC68332 CPU32 test

- check_eprom

  EPROM Test

- check_ram

  RAM test

- check_dpm

  Dual Port Memory test

- check_ipms

  INTERBUS controller test

During POST the diagnostic LEDs are used to display the current status.

Diagnostic Routine	**Diagnostic LEDs**				
	RDY/RUN	FAIL	BSA	PF	HF
Power-on / Reset	0	0	0	0	0
Start	1	1	1	1	1
m68000_self_test	0	1	0	0	0
check_eprom	0	0	1	1	1
check_ram	0	0	1	1	0
check_dpm	0	0	0	1	1
check_ipms	0	0	0	1	0
Initialization	0	0	0	0	0
Diagnosis Done	1-0-…	0	0	0	0

Figure 9-2 : Diagnostic LEDs during POST

10 Diagnostic LEDs on Transition Module

Five LEDs are located on the TIP811-TM-10 Transition Module to support quick diagnosis of the current mode of operation.

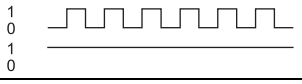
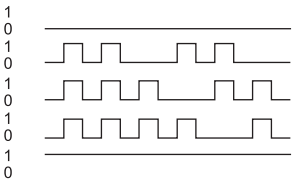
LED	Color	Explanation	Display
RDY/RUN	Green	Ready Run	
FAIL	Red	No Error Remote Bus Error Local Bus Error Controller Error Watchdog or HW Error	
BSA	Yellow	Bus Segment Switched Off	
PF	Yellow	Module Error	
HF	Yellow	Host Error	

Figure 10-1 : Diagnostic LEDs on Transition Module

11 New Commands and Messages

11.1 New Commands

The following new commands are supported by the firmware version 1.1 of the TIP811:

Code	Service-Name
0x0047	Enable_All_Messages
0x0048	Disable_All_Messages
0x0053	Receive_KBL
0x0054	Init_Communication
0x0057	Receive_Communication_Reference
0x0059	InterBus_Delay
0x0081	Var_Read_Request
0x0082	Var_Write_Request
0x0083	Start_Request
0x0084	Stop_Request
0x0085	Information_Report_Request
0x0086	Status_Request
0x0087	Identify_Request
0x0088	Get_OV_Request
0x008B	Initiate_Request
0x008D	Abort_Request
0x00A1	Var_Read_Response
0x00A2	Var_Write_Response
0x00A3	Start_Response
0x00A4	Stop_Response
0x00AB	Initiate_Response
0x00AC	Initiate_Err_Response
0x0112	Read_KBL_Loc_Req
0x0128	Read_KBL_Loc_Req_V24
0x012D	Create_Default_CRL_Req

Figure 11-1: New Commands

11.2 New Messages

The following new messages are supported by the firmware version 1.1 of the TIP811:

Code	Service-Name
0x0065	Too_Many_K_Module_Ind
0x0066	Receive_KR_Error_Con
0x00D6	Quit_Enable_All_Messages_Con
0x00D7	Quit_Disable_All_Messages_Con
0x00E8	Quit_Receive_KBL_Con
0x00E9	Quit_Init_Communication_Con
0x00EB	Quit_Receive_KR_Con
0x00EC	Quit_Bus_Delay_Con
0x00F0	Init_Communication_Not_OK_Con
0x80F1	KBL_Not_OK_Con
0x811B	Read_KBL_Loc_Con
0x8123	Create_Default_CRL_Con
0x8181	Read_Confirmation
0x8182	Write_Confirmation
0x8183	Start_Confirmation
0x8184	Stop_Confirmation
0x8186	Status_Confirmation
0x8187	Identify_Confirmation
0x8188	Get_OV_Confirmation
0x818B	Initiate_Confirmation
0x818C	Initiate_Err_Confirmation
0x81A1	Read_Indication
0x81A2	Write_Indication
0x81A3	Start_Indication
0x81A4	Stop_Indication
0x81A5	Information_Report_Indication
0x81AB	Initiate_Indication
0x81AD	Abort_Indication
0x81AE	Reject_Indication

Figure 11-2: New Messages

12 Important Notes

The hardware of the TIP811-10 INTERBUS Master Interface from TEWS TECHNOLOGIES is based on the original Master Board IBS MA/B-T from PHOENIX CONTACT. The Master Board IBS MA/B-T is a Generation 3 (G3) Controller Board.

The original firmware from PHOENIX CONTACT is running on the TIP811-10.

Version V1.0 of the firmware running on the TIP811-10 Rev. A supports only bit controlled command execution.

Version 1.1 running on the TIP811-10 Rev. B supports the following additional features:

- handshake controlled communication by mailboxes
- up to 32 INTERBUS PCP modules with PCP1.5 (1 word PCP)
- support for the IBS CMD INTERBUS configuration software (PHOENIX CONTACT).

Please note that with the firmware version V1.1 the name of the original PHOENIX CONTACT controller board hardware is changed from IBS MA/B-T to IBS MA/R-T.

For First Time Buyers the Engineering Documentation TIP811-ED is required. This documentation includes the following manuals:

1. **TIP811-DOC** User Manual for the TIP811-10
2. **TIP811-ED** Engineering Manual for the TIP811-10 includes schematics and assembly drawings
   a. **INTERBUS Master Implementation Guide IBS MIG Part 1 UM E** : INTERBUS System Data (a general description of the INTERBUS and cabling instructions)
   b. **INTERBUS Master Implementation Guide IBS MIG Part 2 UM E** : Hardware G3 Controller Board (IBS MA/B-T hardware description)
   c. **INTERBUS Master Implementation Guide IBS MIG Part 3 UM E Manual 1**: Firmware G3 Controller Board (IBS MA/B-T firmware description and description of INTERBUS commands)
   d. **INTERBUS Master Implementation Guide IBS MIG Part 3 UM E Manual 2**: Firmware G3 Controller Board (IBS MA/B-T description of INTERBUS Messages)
   e. INTERBUS Introduction into the Peripherals Communication Protocol (PCP) IBS PCP UM E

The manuals listed under 2a. to 2d. only describe the IBS MA/B-T with the firmware version V1.0. The manual listed under 2e. describes the Peripheral Communication Protocol (PCP 1.5) supported by firmware version V1.1. The TIP811-DOC User Manual (this manual) provides a list of all new commands and messages supported by the firmware version V1.1.

13 Pin Assignment – I/O Connector

Pin	Function
1-25	Not Connected
26	+5V
27	+5V
28	GND
29	INTERBUS Data In (TTL Input)
30	GND
31	INTERBUS Data Out (TTL Output)
32	GND
33	INTERBUS Enable Receiver (TTL Output)
34	GND
35	V.24 TXD (TTL Output)
36	V.24 RTS (TTL Output)
37	V.24 RXD (TTL Input)
38	V.24 CTS (TTL Input)
39	Not Connected
40	Not Connected
41	GND
42	SSI 68332 SCK (TTL Output)
43	+5V
44	SSI 68332 MOSI (TTL Output)
45	GND
46	SSI 68332 MISO (TTL Input)
47	+5V
48	SSI 68332 PCS2 (TTL Output)
49	GND
50	SSI 68332 PCS3 (TTL Output)

Figure 13-1: Pin Assignment I/O Connector

14 Pin Assignment - Transition Module Connectors

14.1 DB9 Female INTERBUS Remote Bus

Pin	Signal	Level
1	INTERBUS Remote Bus DATA OUT +	RS422
2	INTERBUS Remote Bus DATA IN +	RS422
3	Not Connected	
4	Not Connected	
5	Not Connected	
6	INTERBUS Remote Bus DATA OUT -	RS422
7	INTERBUS Remote Bus DATA IN -	RS422
8	Not Connected	
9	Not Connected	

Figure 14-1: DB9 Female INTERBUS Remote Bus

14.2 DB9 Male V.24 Interface (RS232)

Pin	Signal	Level
1	Not Connected	
2	TXD	RS232
3	RXD	RS232
4	Not Connected	
5	GND	
6	Not Connected	
7	RTS	RS232
8	CTS	RS232
9	Not Connected	

Figure 14-2: DB9 Male V.24 Interface (RS232)