*The Embedded I/O Company*

TEWS TECHNOLOGIES

# TPMC700

## 32/16 Digital Outputs (24V, 0.5A)

## High Side Switches

Version 1.1

## User Manual

Issue 1.3

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## TPMC700-10

32 digital outputs front panel I/O

## TPMC700-11

16 digital outputs front panel I/O

## TPMC700-20

32 digital outputs P14 I/O

## TPMC700-21

16 digital outputs P14 I/O



### Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

| | |
|---|---|
| W | Write Only |
| R | Read Only |
| R/W | Read/Write |
| R/C | Read/Clear |
| R/S | Read/Set |



| Issue | Description | Date |
|---|---|---|
| 1.0 | First Issue | September 1999 |
| 1.1 | General Revision | April 2003 |
| 1.2 | Description of optical isolation corrected | March 2004 |
| 1.3 | Added differences of V1.1 | June 2005 |

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# 1 Product Description

The PMC compatible module TPMC700 has 32 (16) digital outputs with galvanic isolation via optocouplers. All outputs resist short-circuits and are protected against thermal overload. The output drivers are capable of driving 0.5A continuous per channel as high side switch. A hardware watchdog clears all outputs in case of trigger failure.

The TPMC700-1x provides front panel I/O with a HD50 SCSI-2 type connector, the TPMC700-2x provides P14 I/O.

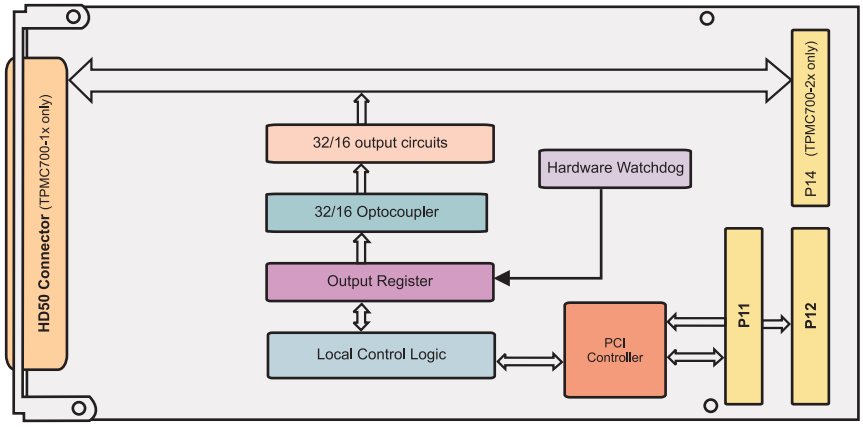


Figure 1-1 : Block Diagram

# 2 Technical Specification

| | | |
|---|---|---|
| **PMC Interface** | | |
| **Mechanical Interface** | PCI Mezzanine Card (PMC) Interface<br>Single Size | |
| **Electrical Interface** | PCI Rev. 2.1 compliant<br>33 MHz / 32 bit PCI<br>3.3V and 5V PCI Signaling Voltage | |
| **On Board Devices** | | |
| **PCI Target Chip** | PCI9030 (PLX Technology) | |
| | | |
| **I/O Interface** | | |
| **Number of Outputs** | TPMC700-10/-20: 32 digital outputs<br>TPMC700-11/-21: 16 digital outputs | |
| **Output Isolation** | Optocouplers for galvanic isolation between system ground and output lines | |
| **External Output Voltage** | 24V DC typical, 6V DC minimum, 48V DC maximum | |
| **Output Current** | 0.5A typical (0.3A for voltages over 32V) | |
| **Short Circuit Current** | 0.8A typical | |
| **Output Voltage Drop** | 1.1V typical @0.5A | |
| **Output Protection** | Overload, short circuit, GND and Vs open wire protection, thermal shutdown | |
| **Watchdog** | Maximum trigger distance = 120ms | |
| **I/O Connector** | TPMC700-10/-11: HD50 SCSI-2 type connector (AMP 787395-5)<br>TPMC700-20/-21: PMC P14 I/O (64 pin Mezzanine Connector) | |
| **Physical Data** | | |
| **Power Requirements** | 130 mA typical @ +3.3V DC | |
| **Temperature Range** | Operating<br>Storage | -25 °C to +85 °C<br>-55°C to +125°C |
| **MTBF** | TPMC700-10: 310 000h<br>TPMC700-11: 449 000h<br>TPMC700-20: 310 000h<br>TPMC700-21: 449 000h | |
| **Humidity** | 5 – 95 % non-condensing | |
| **Weight** | 70 g | |

Figure 2-1 : Technical Specification

# 3 Local Space Addressing

## 3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

| PCI9030 Local Space | PCI9030 PCI Base Address (Offset in PCI Configuration Space) | PCI Space Mapping | Size (Byte) | Port Width (Bit) | Endian Mode | Description |
|---|---|---|---|---|---|---|
| 0 | 2 (0x18) | MEM | 16 | 32 | BIG | CPLD Register Space |
| 1 | 3 (0x1C) | - | - | - | - | Not Used |
| 2 | 4 (0x20) | - | - | - | - | Not Used |
| 3 | 5 (0x24) | - | - | - | - | Not Used |

Figure 3-1 : PCI9030 Local Space Configuration

## 3.2 CPLD Register Space

**PCI Base Address:** **PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).**

| Offset to PCI Base Address 2 | Register Name | Size (Bit) |
|---|---|---|
| 0x0000 | Data Output Register | 32 |
| 0x0004 | Control Register | 32 |

Figure 3-2 : CPLD Register Space

### 3.2.1 Data Output Register

The Data Output Register is a long word wide read/write register used to set or clear the outputs lines.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 31:0 | OUTPUT 32<br>…<br>OUTPUT 1 | Set or clear the corresponding output line<br>1 = active<br>0 = inactive<br>Bit 0 represents OUTPUT 1 …. Bit 31 represents OUTPUT 32 | R/W | 0 |

Figure 3-3 : Data Output Register

**After power-on or reset the Data Output Register is cleared to '0', all outputs are inactive.**

### 3.2.2 Control Register

The Control Register is a 32 bit read/write register.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 31:4 | - | Reserved (0 for reads) | - | 0 |
| 3 | WDOG_STAT | Watchdog Status bit<br>1 = indicate that the watchdog has recognized a failure and has disabled all output channels. The Output Register is locked. Writing '1' to this bit unlocks the Output Register.<br>0 = signals normal operation | R/W | 0 |
| 2 | - | Reserved (0 for reads) | - | 0 |
| 1 | WDOG_EN | Watchdog Enable bit for all 32 outputs<br>1 = enable watchdog function<br>0 = disable | R/W | 0 |
| 0 | - | Reserved (0 for reads) | - | 0 |

Figure 3-4 : Control Register

**The watchdog status is only active if the watchdog is enabled.**

# 4 PCI9030 Target Chip

## 4.1 PCI Configuration Registers (PCR)

### 4.1.1 PCI9030 Header

| PCI CFG Register Address | Write '0' to all unused (Reserved) bits | | | | PCI writeable | Initial Values (Hex Values) |
|---|---|---|---|---|---|---|
| | 31 24 | 23 16 | 15 8 | 7 0 | | |
| 0x00 | Device ID | | Vendor ID | | N | 02BC 1498 |
| 0x04 | Status | | Command | | Y | 0280 0000 |
| 0x08 | Class Code | | | Revision ID | N | 118000 00 |
| 0x0C | BIST | Header Type | PCI Latency Timer | Cache Line Size | Y[7:0] | 00 00 00 00 |
| 0x10 | PCI Base Address 0 for MEM Mapped Config. Registers | | | | Y | FFFFFF80 |
| 0x14 | PCI Base Address 1 for I/O Mapped Config. Registers | | | | Y | FFFFFF81 |
| 0x18 | PCI Base Address 2 for Local Address Space 0 | | | | Y | FFFFFFF0 |
| 0x1C | PCI Base Address 3 for Local Address Space 1 | | | | Y | 00000000 |
| 0x20 | PCI Base Address 4 for Local Address Space 2 | | | | Y | 00000000 |
| 0x24 | PCI Base Address 5 for Local Address Space 3 | | | | Y | 00000000 |
| 0x28 | PCI CardBus Information Structure Pointer | | | | N | 00000000 |
| 0x2C | Subsystem ID | | Subsystem Vendor ID | | N | 000A 1498 |
| 0x30 | PCI Base Address for Local Expansion ROM | | | | Y | 00000000 |
| 0x34 | Reserved | | | New Cap. Ptr. | N | 000000 40 |
| 0x38 | Reserved | | | | N | 00000000 |
| 0x3C | Max_Lat | Min_Gnt | Interrupt Pin | Interrupt Line | Y[7:0] | 00 00 01 00 |
| 0x40 | PM Cap. | | PM Nxt Cap. | PM Cap. ID | N | 4801 00 01 |
| 0x44 | PM Data | PM CSR EXT | PM CSR | | Y | 00 00 0000 |
| 0x48 | Reserved | HS CSR | HS Nxt Cap. | HS Cap. ID | Y[23:16] | 00 00 00 06 |
| 0x4C | VPD Address | | VPD Nxt Cap. | VPD Cap. ID | Y[31:16] | 0000 00 03 |
| 0x50 | VPD Data | | | | Y | 00000000 |

Figure 4-1 : PCI9030 Header

### 4.1.2 PCI Base Address Initialization

**PCI Base Address Initialization is scope of the PCI host software.**

**PCI9030 PCI Base Address Initialization:**

1. Write 0xFFFF_FFFF to the PCI9030 PCI Base Address Register.
2. Read back the PCI9030 PCI Base Address Register.
3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space.

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage.

   Bit 0 = ‘0’: Expansion ROM not used

   Bit 0 = ‘1’: Expansion ROM used
4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to ‘1’, the PCI9030 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).
5. Determine the base address and write the base address to the PCI9030 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9030 PCI Base Address Register.

**After programming the PCI9030 PCI Base Address Registers, the software must enable the PCI9030 for PCI I/O and/or PCI Memory Space access in the PCI9030 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9030, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9030, set bit 1 to '1'.**

| Offset in Config. | Description | Usage |
|---|---|---|
| 0x10 | PCI9030 LCR’s MEM | Used |
| 0x14 | PCI9030 LCR’s I/O | Used |
| 0x18 | PCI9030 Local Space 0 | Used |
| 0x1C | PCI9030 Local Space 1 | Not used |
| 0x30 | Expansion ROM | Not used |

Figure 4-2 : PCI9030 PCI Base Address Usage

## 4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

**The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).**

**Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.**

| Offset from PCI Base Address | Register | Value | Description |
|---|---|---|---|
| 0x00 | Local Address Space 0 Range | 0x0FFF_FFF0 | |
| 0x04 | Local Address Space 1 Range | 0x0000_0000 | |
| 0x08 | Local Address Space 2 Range | 0x0000_0000 | |
| 0x0C | Local Address Space 3 Range | 0x0000_0000 | |
| 0x10 | Local Exp. ROM Range | 0x0000_0000 | |
| 0x14 | Local Re-map Register Space 0 | 0x0000_0001 | |
| 0x18 | Local Re-map Register Space 1 | 0x0000_0000 | |
| 0x1C | Local Re-map Register Space 2 | 0x0000_0000 | |
| 0x20 | Local Re-map Register Space 3 | 0x0000_0000 | |
| 0x24 | Local Re-map Register ROM | 0x0000_0000 | |
| 0x28 | Local Address Space 0 Descriptor | 0x1581_20A0 | |
| 0x2C | Local Address Space 1 Descriptor | 0x0000_0000 | |
| 0x30 | Local Address Space 2 Descriptor | 0x0000_0000 | |
| 0x34 | Local Address Space 3 Descriptor | 0x0000_0000 | |
| 0x38 | Local Exp. ROM Descriptor | 0x0000_0000 | |
| 0x3C | Chip Select 0 Base Address | 0x0000_0009 | |
| 0x40 | Chip Select 1 Base Address | 0x0000_0002 | |
| 0x44 | Chip Select 2 Base Address | 0x0000_0002 | |
| 0x48 | Chip Select 3 Base Address | 0x0000_0002 | |
| 0x4C | Interrupt Control/Status | 0x0000 | |
| 0x4E | EEPROM Write Protect Boundary | 0x0030 | |
| 0x50 | Miscellaneous Control Register | 0x0078_0000 | |
| 0x54 | General Purpose I/O Control | 0x0020_06D2 | |
| 0x70 | Hidden1 Power Management data select | 0x0000_0000 | |
| 0x74 | Hidden 2 Power Management data scale | 0x0000_0000 | |

Figure 4-3 : PCI9030 Local Configuration Register

# 4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

| Address | Offset | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 0x00 | 0x02 | 0x04 | 0x06 | 0x08 | 0x0A | 0x0C | 0x0E |
| 0x00 | 0x02BC | 0x1498 | 0x0280 | 0x0000 | 0x1180 | 0x0000 | s.b. | 0x1498 |
| 0x10 | 0x0000 | 0x0040 | 0x0000 | 0x0100 | 0x4801 | 0x0001 | 0x0000 | 0x0000 |
| 0x20 | 0x0000 | 0x0006 | 0x0000 | 0x0003 | 0x0FFF | 0xFFF0 | 0x0000 | 0x0000 |
| 0x30 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0001 |
| 0x40 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 |
| 0x50 | 0x1581 | 0x20A0 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 |
| 0x60 | 0x0000 | 0x0000 | 0x0000 | 0x0009 | 0x0000 | 0x0002 | 0x0000 | 0x0002 |
| 0x70 | 0x0000 | 0x0002 | 0x0030 | 0x0000 | 0x0078 | 0x0000 | 0x0020 | 0x06D2 |
| 0x80 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0x90 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xA0 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xB0 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xC0 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xD0 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xE0 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |
| 0xF0 | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF | 0xFFFF |

Figure 4-4 : Configuration EEPROM TPMC700-xx

Subsystem-ID Value (Offset 0x0C):

| | |
|---|---|
| TPMC700-10 | 0x000A |
| TPMC700-11 | 0x000B |
| TPMC700-20 | 0x0014 |
| TPMC700-21 | 0x0015 |

## 4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

**CNTRL[30] PCI Adapter Software Reset:**

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

# 5 Configuration Hints

## 5.1 Big / Little Endian

- PCI – Bus (Little Endian)

| | |
|---|---|
| Byte 0 | AD[7..0] |
| Byte 1 | AD[15..8] |
| Byte 2 | AD[23..16] |
| Byte 3 | AD[31..24] |

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

| **Big Endian** | | **Little Endian** | |
|---|---|---|---|
| **32 Bit** | | **32 Bit** | |
| Byte 0 | D[31..24] | Byte 0 | D[7..0] |
| Byte 1 | D[23..16] | Byte 1 | D[15..8] |
| Byte 2 | D[15..8] | Byte 2 | D[23..16] |
| Byte 3 | D[7..0] | Byte 3 | D[31..24] |
| **16 Bit upper lane** | | **16 Bit** | |
| Byte 0 | D[31..24] | Byte 0 | D[7..0] |
| Byte 1 | D[23..16] | Byte 1 | D[15..8] |
| **16 Bit lower lane** | | | |
| Byte 0 | D[15..8] | | |
| Byte 1 | D[7..0] | | |
| **8 Bit upper lane** | | **8 Bit** | |
| Byte 0 | D[31..24] | Byte 0 | D[7..0] |
| **8 Bit lower lane** | | | |
| Byte 0 | D[7..0] | | |

Figure 5-1 : Local Bus Little/Big Endian

**Standard use of the TPMC700:**

| | |
|---|---|
| Local Address Space 0 | 32 bit bus in Big Endian Mode |
| Local Address Space 1 | not used |
| Local Address Space 2 | not used |
| Local Address Space 3 | not used |
| Expansion ROM Space | not used |

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

For further information please refer to the PCI9030 manual which is also part of the TPMC700-ED Engineering Documentation.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

| Short cut | Offset | Name |
|---|---|---|
| LAS0BRD | 0x28 | Local Address Space 0 Bus Region Description Register |
| LAS1BRD | 0x2C | Local Address Space 0 Bus Region Description Register |
| LAS2BRD | 0x30 | Local Address Space 0 Bus Region Description Register |
| LAS3BRD | 0x34 | Local Address Space 0 Bus Region Description Register |
| EROMBRD | 0x38 | Expansion ROM Bus Region Description Register |

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

# 6 Functional Description of Digital Outputs

## 6.1 Optical Isolation

The TPMC700 has 32 (TPMC700-10/-20) or 16 (TPMC700-11/-21) digital outputs. The standard signal level for these outputs is 24V DC. All outputs are isolated by optocouplers from the system and in two groups (output OUT1-16 against output OUT17-32) against each other.

Within these two groups there are four subgroups for the VS power supply which allow different supply voltages in groups of four, but referenced to the same GND.

| Group | VS/standard 24V DC | Ground | Input |
|---|---|---|---|
| O 1 | VS_O1 | GND_OA | OUT 1<br>OUT 2<br>OUT 3<br>OUT 4 |
| O 2 | VS_ O2 | | OUT 5<br>OUT 6<br>OUT 7<br>OUT 8 |
| O 3 | VS_ O3 | | OUT 9<br>OUT 10<br>OUT 11<br>OUT 12 |
| O 4 | VS_ O4 | | OUT 13<br>OUT 14<br>OUT 15<br>OUT 16 |
| O 5 | VS_ O5 | GND_OB | OUT 17<br>OUT 18<br>OUT 19<br>OUT 20 |
| O 6 | VS_ O6 | | OUT 21<br>OUT 22<br>OUT 23<br>OUT 24 |
| O 7 | VS_ O7 | | OUT 25<br>OUT 26<br>OUT 27<br>OUT 28 |
| O 8 | VS_ O8 | | OUT 29<br>OUT 30<br>OUT 31<br>OUT 32 |

Figure 6-1 : Isolated Digital Outputs

## 6.2 Output Polarity

Each output can be individually switched to the according power supply VS_Ox (high side switch).

## 6.3 Overload Protection

The output drivers used on the TPMC700 are ‘smart drivers’ TDE1707. The maximum continuous output current is 0.5A. The output circuits are protected against overload, short circuit and over temperature. In case of such failure the corresponding output is switched off until the error condition is removed. The output returns automatically to normal operation, i.e. the state programmed in the Data Output Register.

For details about the protection of the TDE1707 please refer to the data sheet which is part of the TPMC700-ED Engineering Documentation.

## 6.4 Output Watchdog

Writing ‘1’ into bit 1 of the Global Control Register the hardware watchdog function is enabled. The status of the watchdog is indicated at bit 3 of the Global Control Register.

Any software accesses (read or write) to the Data Output Register will retrigger the watchdog. The maximum time between two accesses is set to 120ms. If the time expires without a software access all outputs go into “OFF” state. At the same time the watchdog status will change from ‘0’ to ‘1’ and locks the Data Output Register. This prevents a write access to the Data Output Register.

Writing ‘1’ to the watchdog status (bit 3 Control Register) clears this bit and also unlocks the Output Register. After unlocking the Data Output Register the output stays in the “OFF” state till the next write access to this register.

**The watchdog is disabled after power-on or reset.**

# 7 Programming Hints

## 7.1 Local Read/Write

The local CPLD register design is developed for a long word (32 bit) read/write access. A byte or word access will fail.

**Use only long word read/write accesses to the TPMC700.**

# 8 Installation

## 8.1 Output Wiring

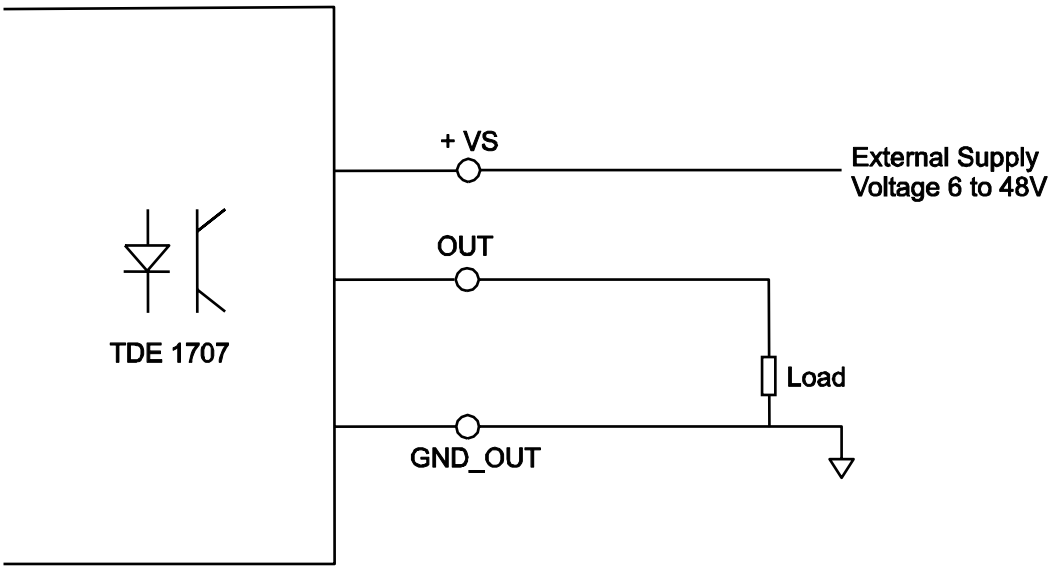


Figure 8-1 : Output Wiring as High Side Switch

# 9 Pin Assignment

## 9.1 Front panel HD50 SCSI-2 type connector

| Pin | Function |
|---|---|
| 1 | VS_O1 |
| 2 | VS_O1 |
| 3 | VS_O2 |
| 4 | VS_O2 |
| 5 | VS_O3 |
| 6 | VS_O3 |
| 7 | VS_O4 |
| 8 | VS_O4 |
| 9 | VS_O5 |
| 10 | VS_O5 |
| 11 | VS_O6 |
| 12 | VS_O6 |
| 13 | VS_O7 |
| 14 | VS_O7 |
| 15 | VS_O8 |
| 16 | VS_O8 |
| 17 | OUT 1 |
| 18 | OUT 2 |
| 19 | OUT 3 |
| 20 | OUT 4 |
| 21 | OUT 5 |
| 22 | OUT 6 |
| 23 | OUT 7 |
| 24 | OUT 8 |
| 25 | OUT 9 |

| Pin | Function |
|---|---|
| 26 | OUT 10 |
| 27 | OUT 11 |
| 28 | OUT 12 |
| 29 | OUT 13 |
| 30 | OUT 14 |
| 31 | OUT 15 |
| 32 | OUT 16 |
| 33 | OUT 17 |
| 34 | OUT 18 |
| 35 | OUT 19 |
| 36 | OUT 20 |
| 37 | OUT 21 |
| 38 | OUT 22 |
| 39 | OUT 23 |
| 40 | OUT 24 |
| 41 | OUT 25 |
| 42 | OUT 26 |
| 43 | OUT 27 |
| 44 | OUT 28 |
| 45 | OUT 29 |
| 46 | OUT 30 |
| 47 | OUT 31 |
| 48 | OUT 32 |
| 49 | GND_OA |
| 50 | GND_OB |

Figure 9-1 : HD50 SCSI-2 type connector

**Please check the maximum current of the used connection cable. Some standard cables (AWG28 50 pol.) are limited to 0.75 A per lead.**

## 9.2 Mezzanine Card Connector P14

| Pin | Function |
|---|---|
| 1 | VS_O1 |
| 2 | VS_O1 |
| 3 | VS_O2 |
| 4 | VS_O2 |
| 5 | VS_O3 |
| 6 | VS_O3 |
| 7 | VS_O4 |
| 8 | VS_O4 |
| 9 | VS_O5 |
| 10 | VS_O5 |
| 11 | VS_O6 |
| 12 | VS_O6 |
| 13 | VS_O7 |
| 14 | VS_O7 |
| 15 | VS_O8 |
| 16 | VS_O8 |
| 17 | OUT 1 |
| 18 | OUT 2 |
| 19 | OUT 3 |
| 20 | OUT 4 |
| 21 | OUT 5 |
| 22 | OUT 6 |
| 23 | OUT 7 |
| 24 | OUT 8 |
| 25 | OUT 9 |
| 26 | OUT 10 |
| 27 | OUT 11 |
| 28 | OUT 12 |
| 29 | OUT 13 |
| 30 | OUT 14 |
| 31 | OUT 15 |
| 32 | OUT 16 |

| Pin | Function |
|---|---|
| 33 | OUT 17 |
| 34 | OUT 18 |
| 35 | OUT 19 |
| 36 | OUT 20 |
| 37 | OUT 21 |
| 38 | OUT 22 |
| 39 | OUT 23 |
| 40 | OUT 24 |
| 41 | OUT 25 |
| 42 | OUT 26 |
| 43 | OUT 27 |
| 44 | OUT 28 |
| 45 | OUT 29 |
| 46 | OUT 30 |
| 47 | OUT 31 |
| 48 | OUT 32 |
| 49 | GND_OA |
| 50 | GND_OB |
| 51 | NC |
| 52 | NC |
| 53 | NC |
| 54 | NC |
| 55 | NC |
| 56 | NC |
| 57 | NC |
| 58 | NC |
| 59 | NC |
| 60 | NC |
| 61 | NC |
| 62 | NC |
| 63 | NC |
| 64 | NC |

Figure 9-2 : Mezzanine Card Connector P14

**Please verify that the tracks from the P14 connector to the Px connector of the PMC carrier board are designed for a current of min. 0.5A per output.**